In the Drawings

The Applicant has submitted proposed drawing amendments for approval by the Examiner. Attached please find a copy of the drawings with red ink markings showing the proposed amendments for which approval of the Examiner is requested, as well as a copy of the drawings that include the proposed amendments.

REMARKS

The Applicants appreciate the Examiner's care and attention in reviewing the present Application and in providing comments in the Office Action. In the Office Action, the Examiner indicated that a new title is required that is clearly indicative of the invention to which the claims are directed. Further, the Examiner objected to the drawings because of inconsistent use of the reference character "514" and with respect to claim 10.

Additionally, the Examiner rejected claims 2, 4, 12, 15, 17 and 21 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Further, the Examiner rejected claims 1, 3-9, 11-16 and 18-21 under 35 U.S.C. 103(a) as being unpatentable over Seale et al. (U.S. Pat. No. 6,208,497) in view of Yamaguchi (Japanese patent document no. 404000907).

The Applicant will address each of these objections and rejections in turn.

OBJECTION TO THE TITLE

In accordance with the Examiner's suggestion, the Applicants have amended the title. The Applicants respectfully submit that the title proposed by the Examiner is excessively long in view of the requirements of 37 CFR 1.72.

As an alternative, the Applicants have instead amended the title to further refer to the employment of an amplifier and a switched feedback resistance. The Applicants respectfully submit that the amended title is clearly indicative of the invention to which the claims are directed. No new matter has been added by this amendment.

OBJECTIONS TO THE DRAWINGS

The Applicants appreciate the Examiner's observation that the reference character "514" is used both to refer to an output port and a second feedback resistor. To rectify this error, the Applicants have amended Fig. 5 so that the output port is labeled with a new reference character "519" rather than "514". The existing reference character "514" continues to be used to refer to the second feedback resistor. Additionally, three paragraphs in the Specification have been amended to correspond properly to the amended Fig. 5 and to correct a minor typographical error. No new matter has been added by these amendments.

As for the Examiner's second comment, in paragraph 3 of the Office Action, that Fig. 5 should be corrected to conform to the language of pending claim 10, the Applicants respectfully traverse this objection. The Applicants submit that the language of pending claim 10 is consistent with the language in the Specification used to describe the element labeled R_{F2} (see, e.g., col. 18, line 15). The Applicants further submit that the Applicants can refer to this element by way of the term "feedback resistor", since it is allowable for the Applicants to be their own lexicographer (see the MPEP at Section 2111.01, third subsection).

REJECTIONS UNDER 35 USC 112

With respect to the Examiner's first ground of rejection under 35 USC 112, which appears to concern pending claim 2, the Applicants respectfully submit that claim 2 is definite as written to include at least one of a field effect transistor, a metal oxide semiconductor field effect transistor, and a bipolar junction transistor. As stated in the Specification at page 17, lines 10-12, for example, any of a number of different switching devices can be employed as element 506 in Fig. 5. Typically, one switching device will be employed as element 506. However, although perhaps not the preferred embodiment, it is nonetheless possible that element 506 could include multiple switching devices at the same time. Thus, the language "at least one of" used in claim 2 is appropriate.

With respect to the Examiner's comment concerning claim 4, the Applicants respectfully submit that use of a formula is supported by the Specification at page 21, lines 20-24, for example. The exact nature of the formulas used in different embodiments will vary depending upon the embodiments. Common among these embodiments, however, will be the usage of a formula that includes two different multiplicative factors (e.g., a factor of ten and a factor of one) depending upon the status of operation of the processor. Such usage of two different multiplicative factors in a formula as claimed is supported by the Specification at page 21, lines 20-29.

As for the Examiner's comment regarding claim 12, the Applicants believe that the Examiner has misunderstood the terms "fourth signal" and "first signal." The fourth signal is a signal, received directly or indirectly from the alternator, that is processed by the current transformation means to generate the first signal. In one embodiment, the current transformation means can be considered to be (or include) the current transformer 158, which receives the

signal from the alternator 154 (e.g., the fourth signal) and in turn produces the signal provided at system current input 225 (e.g., the first signal).

With respect to the Examiner's comment concerning claim 21, the Applicants respectfully submit that the appropriate parameters for measuring current values, and also the standards for excessive heat for alternators, would be known to one skilled in the art of alternator design.

Further with respect to the Examiner's comments concerning claims 4 and 21, the Examiner is referred to copending U.S. patent application no. 09/695,166 entitled "METHOD AND APPARATUS FOR PREVENTING EXCESSIVE HEAT GENERATION IN AN ALTERNATOR OF A GENERATOR SET", which has been incorporated by reference into the present Application (see page 1, line 24 of the Specification).

Finally, although the Examiner has apparently also rejected claims 15 and 17 as being indefinite, the grounds for these rejections are unclear to the Applicants. The Applicants respectfully request that the Examiner clarify the grounds for rejecting claims 15 and 17 as being indefinite, in the event that the above arguments concerning claims 2, 4, 12 and 21 are not applicable also to claims 15 and 17.

REJECTIONS UNDER 35 USC 103(a)

In the 7th paragraph of the Office Action, the Examiner rejected claims 1, 3-9, 11-16 and 18-21 under 35 USC 103(a) as being unpatentable over Seale et al. in view of Yamaguchi. The Applicants respectfully traverse the Examiner's rejection, for several reasons. First, the Applicants respectfully submit that neither of Seale et al. and Yamaguchi apparently relates to the sensing or measuring of alternator current levels, and neither of the references includes the limitations of pending independent claims 1, 11 and 14 that relate to

sensing alternator currents. Additionally, because neither Seale et al. nor Yamaguchi relates to the sensing or measuring of alternator current levels in a genset, and because Seale et al. and Yamaguchi have totally dissimilar purposes with respect to one another, the Applicants cannot identify any suggestion to combine or modify Seale et al. and Yamaguchi to arrive at the present invention. Finally, the Applicants cannot find, in either of Seale et al. or Yamaguchi, any disclosure of certain other limitations within the independent claims.

The Applicants respectfully submit that neither of Seale et al. and Yamaguchi appears to relate to the sensing or measuring of alternator current levels within the alternator of a genset. The Applicants are unable to locate any use of the word "alternator" in either of the references. Consequently, the Applicants submit that Seale et al. and Yamaguchi, both alone and in combination, fail to disclose the limitations in the independent claims 1, 11 and 14 that concern alternators. In particular, these limitations include: in claim 1, "a signal indicative of an alternator current level" and "a current indication related to a level of alternator current"; in claim 11, "a first signal indicative of a current level within the alternator"; and in claim 14, "a first indication of a current level within the alternator".

Rather than relating to the sensing of alternator current levels within the alternator of a genset in order to prevent exposure of the alternator to excessive heat, Seale et al. and Yamaguchi appear to have different purposes, both with respect to the pending invention and with respect to one another. Specifically, Seale et al. appears to relate to complex control circuitry for the servo control of electromagnetic devices, particularly solenoids (see, e.g., col. 1, lines 7-16). Yamaguchi appears to concern a specialized

implementation of an amplifier circuit that reduces amplification error caused by the ON resistance of an analog switch (see the Abstract).

Further, the Applicants are unable to find any discussion in Yamaguchi of employing a switching device to change the gain factor of an amplifier to allow for improved sensing of alternator currents. Indeed, the Applicants are unable to find any rationale within Seale et al. or Yamaguchi for utilizing the amplifier circuit of Yamaguchi within the system of Seale et al. Because Seale et al. and Yamaguchi concern different applications and have purposes that are unrelated to one another, and because neither Seale et al. nor Yamaguchi relates to the sensing of alternator currents in a genset, the Applicants respectfully submit that there is no suggestion to combine or modify Seale et al. and Yamaguchi to arrive at any of the pending independent claims 1, 11 and 14.

Further, Seale et al. and Yamaguchi, both alone and in combination, fail to disclose several other limitations of the independent claims 1, 11 and 14. In particular, the Applicants are unable to find any disclosure in either reference of a processor that is operable to control a switching element so that the switching element is closed when a current indication increases to exceed a first threshold, and so that the switching element is opened when the current indication falls below a second threshold (as in pending claim 1). Similarly, the Applicants are unable to find any disclosure in either reference of switching a status of a switching element to reduce a gain of an amplifier when measured current values increase to exceed a first threshold, and switching the status of the switching element to increase the gain of the amplifier when the measured current values fall below a second threshold (as in pending claim 14). Further, the Applicants are unable to find any disclosure in

either reference that relates to a processing means that both processes a signal output by an amplification means and controls a modification means to adjust the level of amplification of the amplification means. In short, the cited prior art references fail to teach switching of amplifier gain in order to keep measured current signals within a high-sensitivity range of the measurement system.

For all of these reasons, therefore, the Applicants respectfully submit that the pending independent claims 1, 11 and 14 are allowable over Seale et al. in view of Yamaguchi. Further, the Applications respectfully submit that each of pending claims 3-10, 12-13 and 15-21, which respectively depend from claims 1, 11 and 14, also are allowable over the cited prior art references.

* * *

Conclusion

In view of the amendments to the specification and the figures and the Remarks being submitted herewith, and in view of the distinctions between the presently claimed subject matter and the teachings of the cited patents, the Applicant respectfully requests reconsideration and allowance of the present application.

The Applicant wishes to invite the Examiner to telephone the Applicant's attorney at the number listed below if discussion with the Applicant's attorney would be of

assistance to the Examiner or further the prosecution of the present application.

Respectfully submitted,
David A. Hintz et al.

Dated: September 7, 2001

By: 

John T. Pienkos
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QBMKE\5104968.1

VERSION SHOWING CHANGES

In the Specification

Amended paragraph being substituted for the pending paragraph beginning on page 16, line 27 and ending on page 17, line 4:

A second input resistor 515 (R_{I2}) is similarly coupled between a second input port 503 of the operational amplifier 502 and a second input port 509 of the current conditioning circuit 246, which is coupled to a second terminal 157 of the current transformer 158 by way of the system current input 225. A burden resistor 159 (R_B) is coupled between the two terminals 155,157 of the current transformer to provide a return path for current between terminals 155,157. An output port 507 of the operational amplifier 502 is provided to the analog-to-digital converter 248. The output port 507 is coupled to an [outport] **output** port [514] **519** of the current conditioning circuit 246.

Amended paragraph being substituted for the pending paragraph beginning on page 17, line 25 and ending on page 18, line 13:

The current conditioning circuit 246 amplifies the input signal from the current transformer 158 as a conventional differential amplifier. Thus, when the adjustment resistor 508 is not coupled between the first input port 501 and the output port 507 due to the switching element 506 being turned off, the voltage gain experienced between the input port 512 and the output port [514] **519** of the current conditioning circuit 246 is proportional to the ratio of the resistance of the feedback resistor 504 to the resistance of the input

resistor 505 (e.g., R_{F1}/R_I). However, when the adjustment resistor 508 is coupled in parallel with the feedback resistor 504 because the switching element 506 is turned on, the gain of the differential amplifier is proportional to the ratio of the parallel combination of the resistances of the feedback resistor and the adjustment resistor to the resistance of the input resistor 505 $\{R_{A1}R_{F1}/[(R_{A1}+R_{F1})R_I]\}$. Thus, by turning on the switching element 506, the gain of the differential amplifier can be reduced. Further, by appropriately choosing the ratio of R_{A1} to R_{F1}, the gain of the differential amplifier can be reduced by a factor of 10 when the switching element 506 is turned on, in particular.

Amended paragraph being substituted for the pending paragraph at page 19, lines 3-20:

Without the second feedback and adjustment resistors 514,518 and the second switching element 516, the voltage output at port [514] **519** would tend to zero volts for a zero volt differential applied between ports 512 and 509; however, with the second feedback and adjustment resistors and the second switching element the voltage output is biased to 2.5 Volts. By including the second feedback and adjustment resistors 514,518 and second switching element 516, therefore, the output of the differential amplifier is biased to a point above the noise level, and the analog-to-digital converter 248 can be provided power by way of a single positive power supply, instead of requiring both positive and negative power supplies (to handle positive and negative outputs from the differential amplifier. Use of pairs of feedback, adjustment, and input resistors having the same values allows for balanced operation of the differential amplifier.

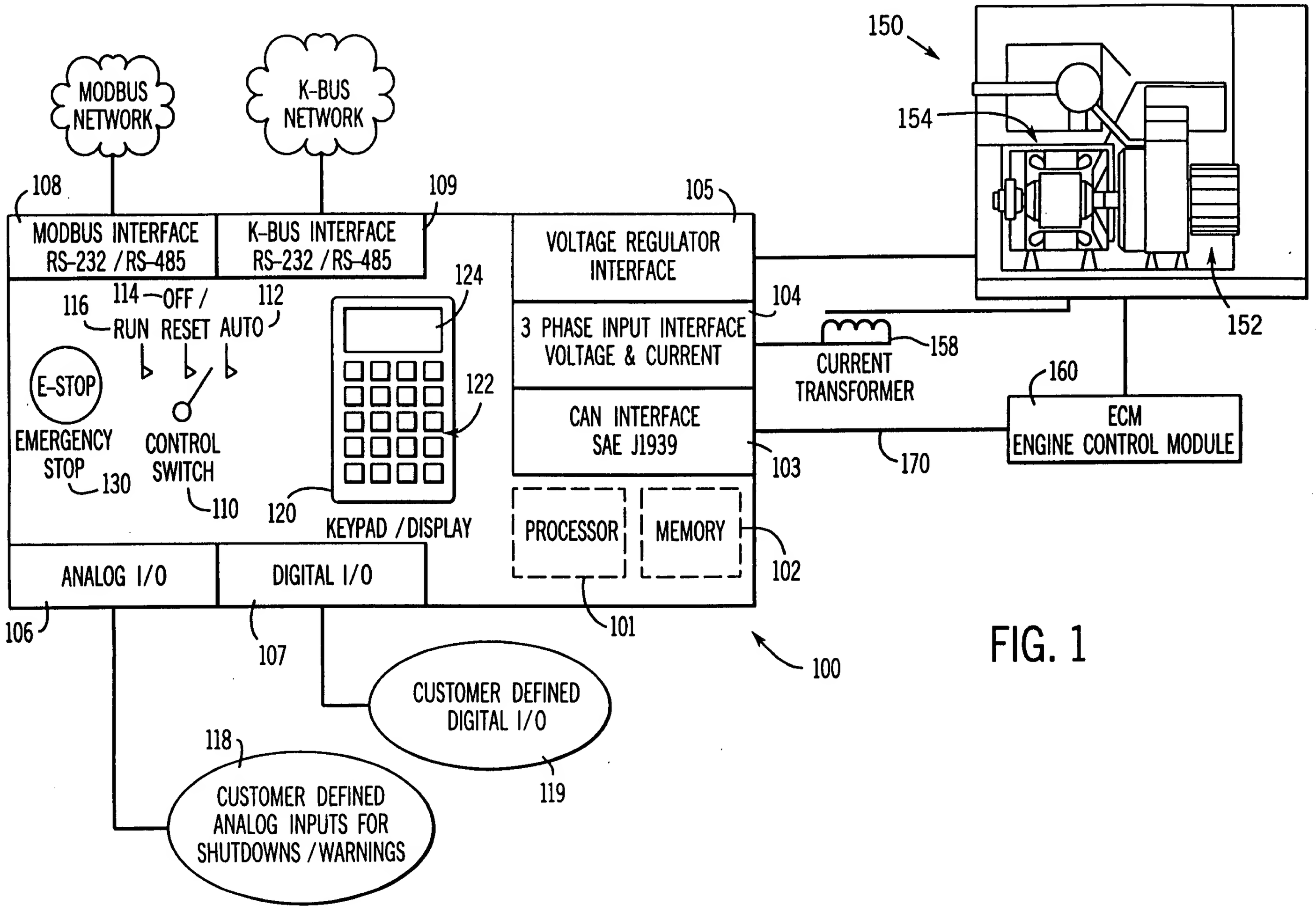
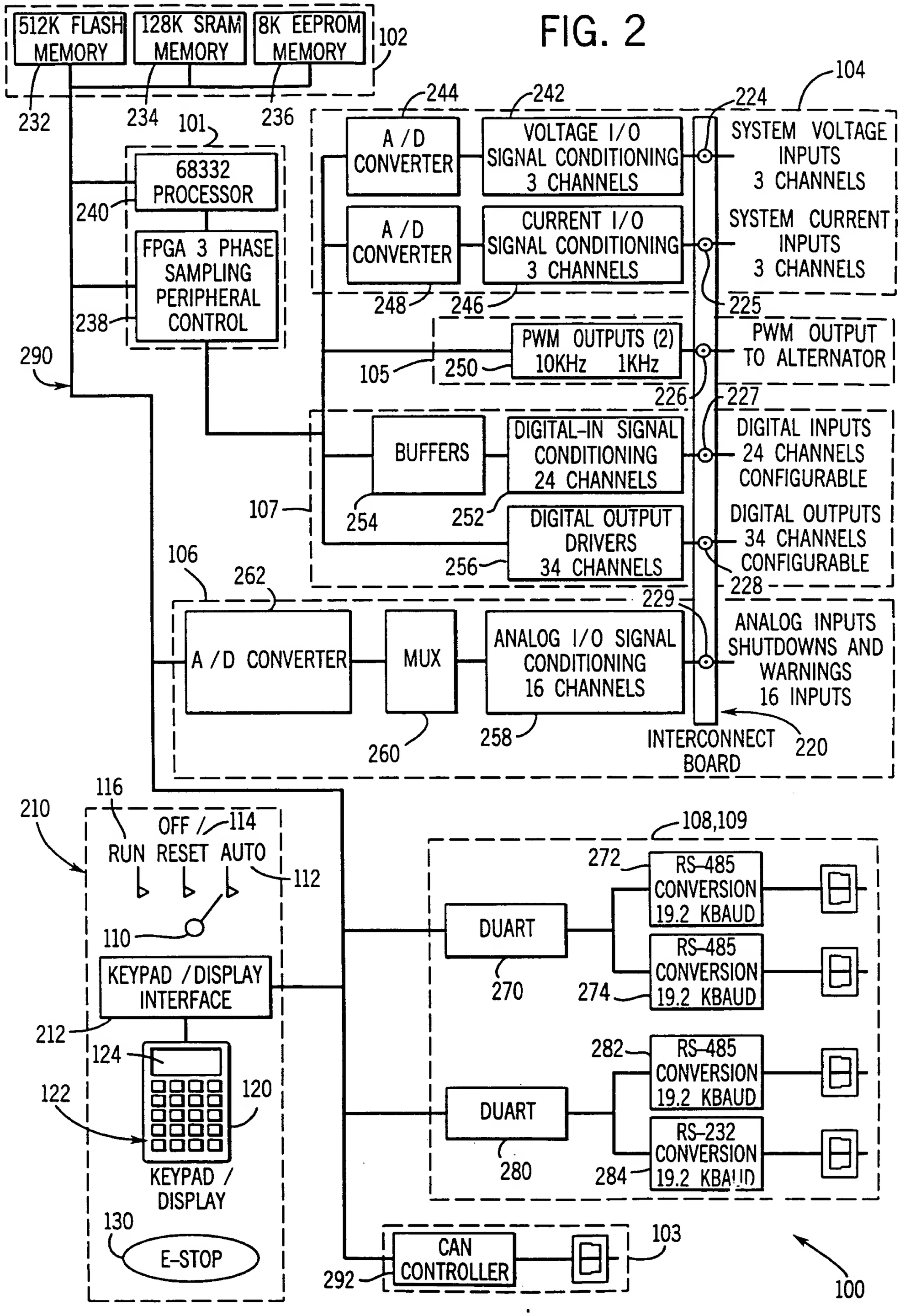

MODBUS NETWORK
K-BUS NETWORK
108
109
105
MODBUS INTERFACE RS-232 / RS-485
K-BUS INTERFACE RS-232 / RS-485
VOLTAGE REGULATOR INTERFACE
104
3 PHASE INPUT INTERFACE VOLTAGE & CURRENT
CAN INTERFACE SAE J1939
103
PROCESSOR
MEMORY
102
101
ANALOG I/O
DIGITAL I/O
106
107
114
OFF /
RUN
RESET
AUTO
112
116
E-STOP
EMERGENCY STOP
130
CONTROL SWITCH
110
124
122
120
KEYPAD / DISPLAY
150
154
152
158
CURRENT TRANSFORMER
160
ECM ENGINE CONTROL MODULE
170
100
CUSTOMER DEFINED DIGITAL I/O
119
118
CUSTOMER DEFINED ANALOG INPUTS FOR SHUTDOWNS / WARNINGS

FIG. 1

FIG. 2


512K FLASH MEMORY
128K SRAM MEMORY
8K EEPROM MEMORY
102
232
234
236
101
68332 PROCESSOR
240
FPGA 3 PHASE SAMPLING PERIPHERAL CONTROL
238
290
104
244
242
224
A / D CONVERTER
VOLTAGE I/O SIGNAL CONDITIONING 3 CHANNELS
SYSTEM VOLTAGE INPUTS 3 CHANNELS
A / D CONVERTER
CURRENT I/O SIGNAL CONDITIONING 3 CHANNELS
SYSTEM CURRENT INPUTS 3 CHANNELS
248
246
225
PWM OUTPUTS (2) 10KHz 1KHz
PWM OUTPUT TO ALTERNATOR
105
250
226
227
BUFFERS
DIGITAL-IN SIGNAL CONDITIONING 24 CHANNELS
DIGITAL INPUTS 24 CHANNELS CONFIGURABLE
107
254
252
DIGITAL OUTPUT DRIVERS 34 CHANNELS
DIGITAL OUTPUTS 34 CHANNELS CONFIGURABLE
256
228
106
262
229
A / D CONVERTER
MUX
ANALOG I/O SIGNAL CONDITIONING 16 CHANNELS
ANALOG INPUTS SHUTDOWNS AND WARNINGS 16 INPUTS
260
258
INTERCONNECT BOARD
220
116
210
OFF
114
RUN RESET AUTO
112
110
108,109
272
RS-485 CONVERSION 19.2 KBAUD
DUART
270
274
RS-485 CONVERSION 19.2 KBAUD
KEYPAD / DISPLAY INTERFACE
212
282
RS-485 CONVERSION 19.2 KBAUD
124
122
120
DUART
280
284
RS-232 CONVERSION 19.2 KBAUD
KEYPAD / DISPLAY
130
E-STOP
CAN CONTROLLER
103
292
100

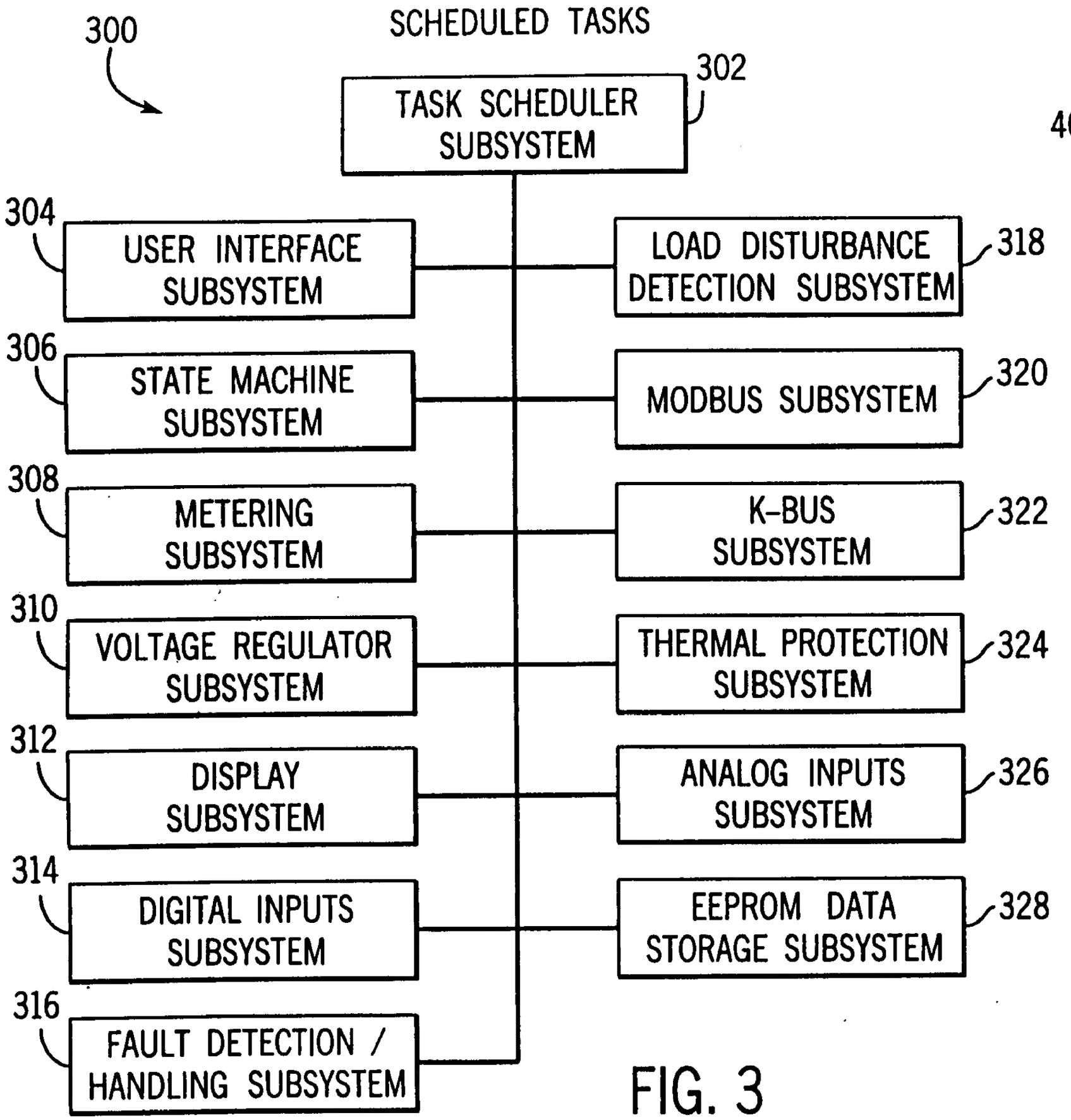

300
SCHEDULED TASKS
TASK SCHEDULER SUBSYSTEM
302
304
USER INTERFACE SUBSYSTEM
306
STATE MACHINE SUBSYSTEM
308
METERING SUBSYSTEM
310
VOLTAGE REGULATOR SUBSYSTEM
312
DISPLAY SUBSYSTEM
314
DIGITAL INPUTS SUBSYSTEM
316
FAULT DETECTION / HANDLING SUBSYSTEM
LOAD DISTURBANCE DETECTION SUBSYSTEM
318
MODBUS SUBSYSTEM
320
K-BUS SUBSYSTEM
322
THERMAL PROTECTION SUBSYSTEM
324
ANALOG INPUTS SUBSYSTEM
326
EEPROM DATA STORAGE SUBSYSTEM
328

FIG. 3

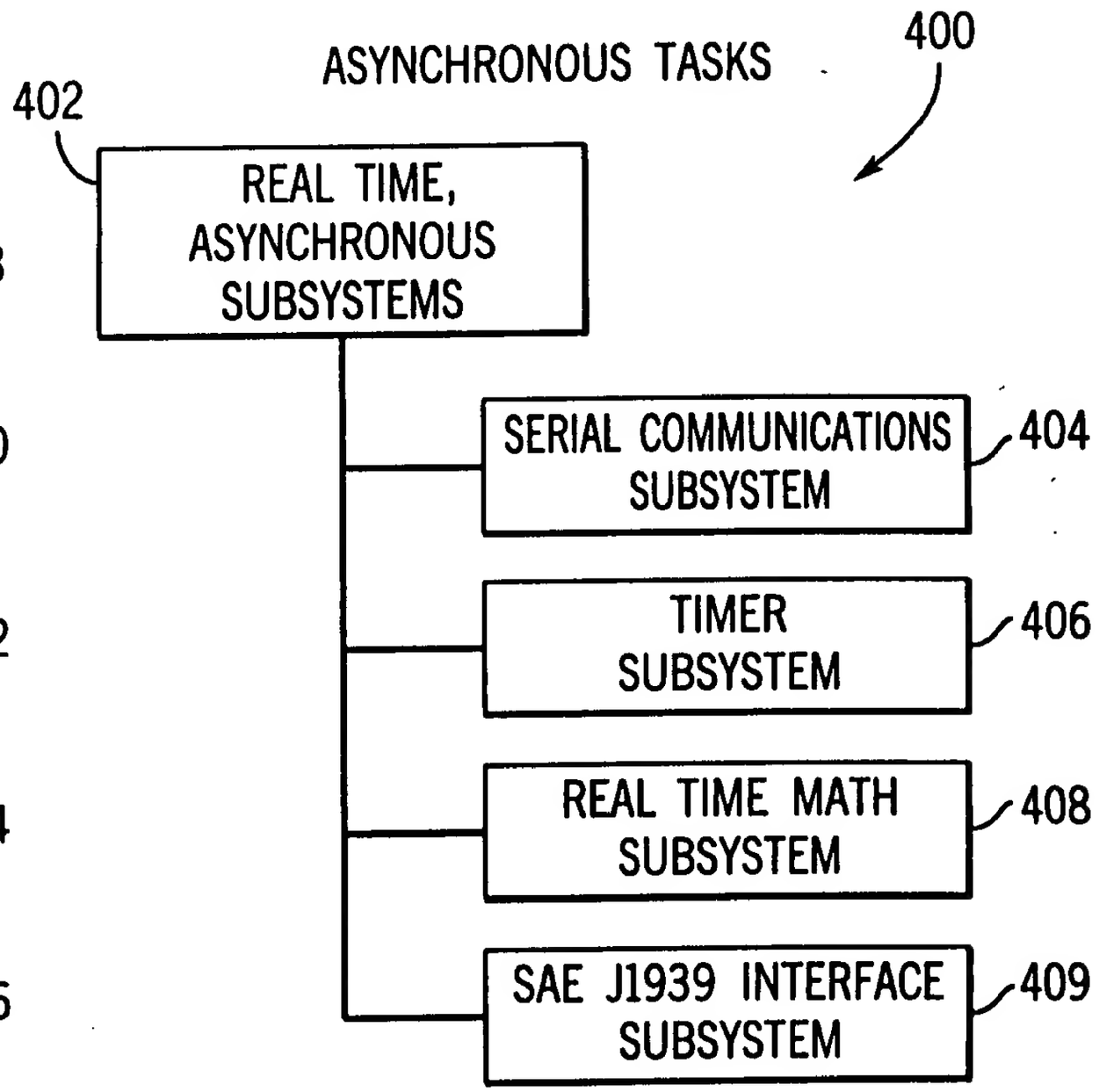
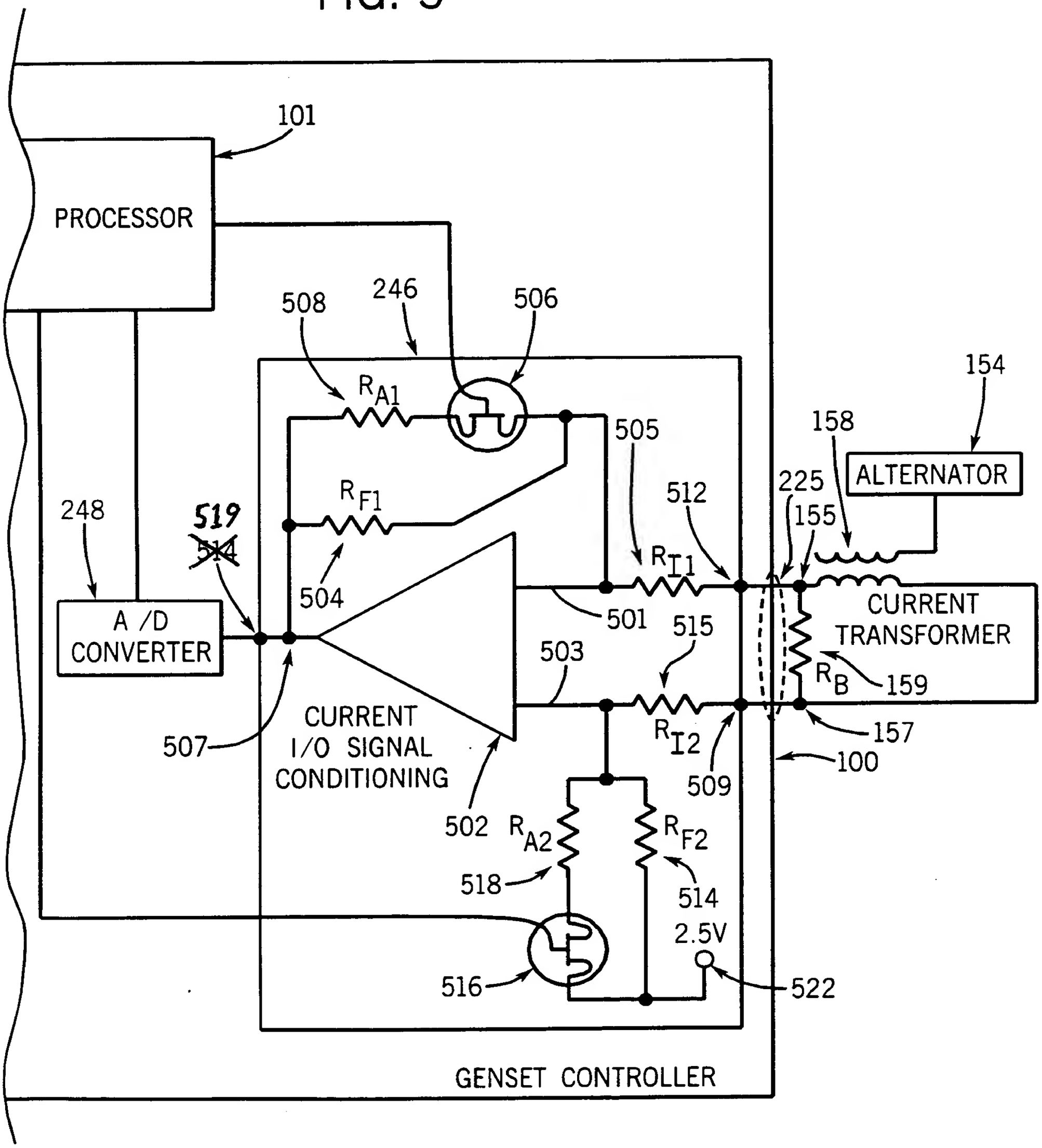

ASYNCHRONOUS TASKS
400
402
REAL TIME, ASYNCHRONOUS SUBSYSTEMS
SERIAL COMMUNICATIONS SUBSYSTEM
404
TIMER SUBSYSTEM
406
REAL TIME MATH SUBSYSTEM
408
SAE J1939 INTERFACE SUBSYSTEM
409

FIG. 4

FIG. 5


101
PROCESSOR
508
246
506
R_{A1}
R_{F1}
505
512
154
158
ALTERNATOR
225
155
248
519
514
504
R_{I1}
501
515
503
CURRENT TRANSFORMER
R_B
159
A /D CONVERTER
507
CURRENT I/O SIGNAL CONDITIONING
R_{I2}
157
100
509
502
R_{A2}
R_{F2}
518
514
2.5V
516
522
GENSET CONTROLLER

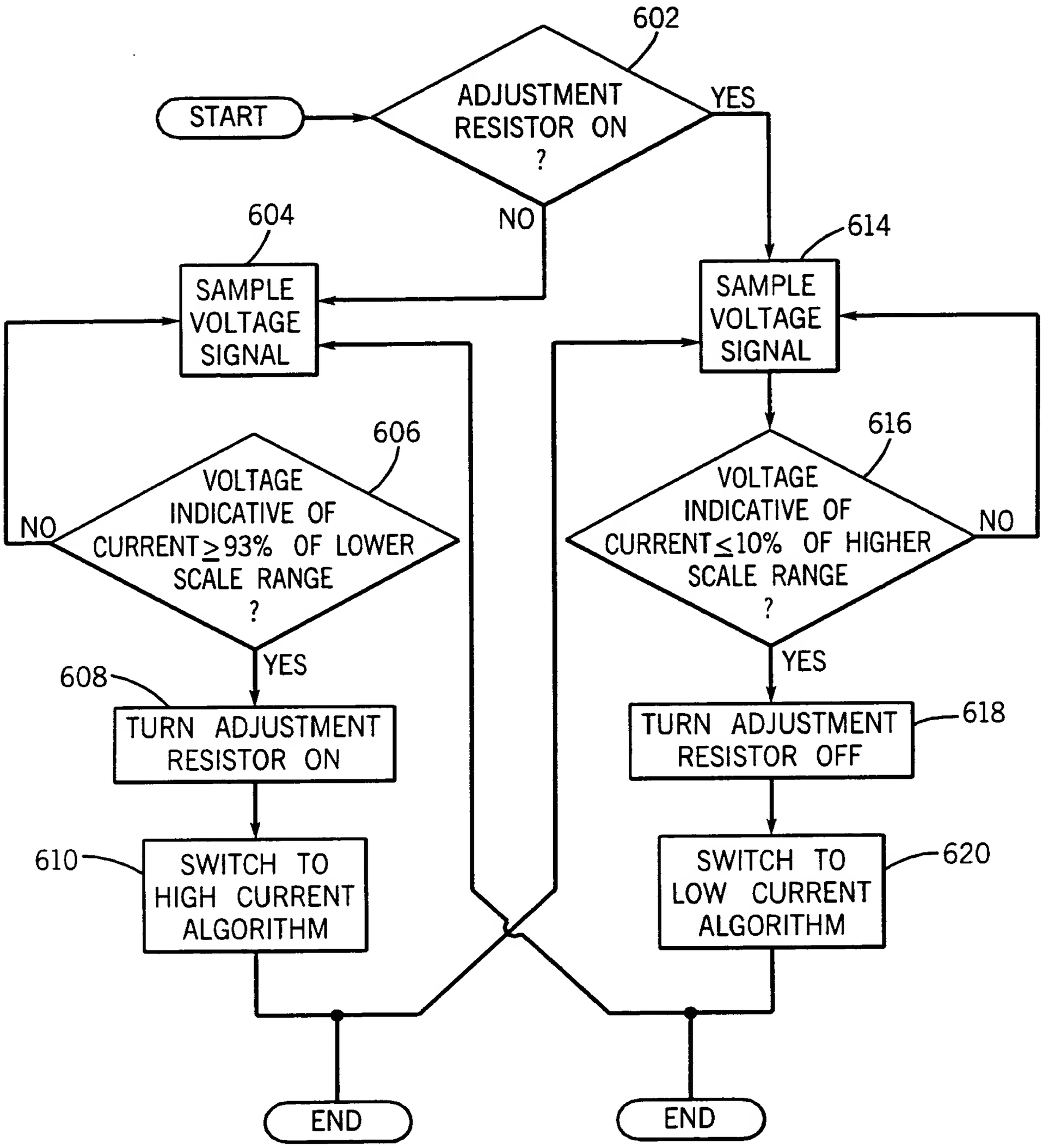

602
START
ADJUSTMENT RESISTOR ON ?
YES
NO
604
SAMPLE VOLTAGE SIGNAL
614
SAMPLE VOLTAGE SIGNAL
606
VOLTAGE INDICATIVE OF CURRENT ≥ 93% OF LOWER SCALE RANGE ?
NO
YES
616
VOLTAGE INDICATIVE OF CURRENT ≤ 10% OF HIGHER SCALE RANGE ?
NO
YES
608
TURN ADJUSTMENT RESISTOR ON
618
TURN ADJUSTMENT RESISTOR OFF
610
SWITCH TO HIGH CURRENT ALGORITHM
620
SWITCH TO LOW CURRENT ALGORITHM
END
END

FIG. 6